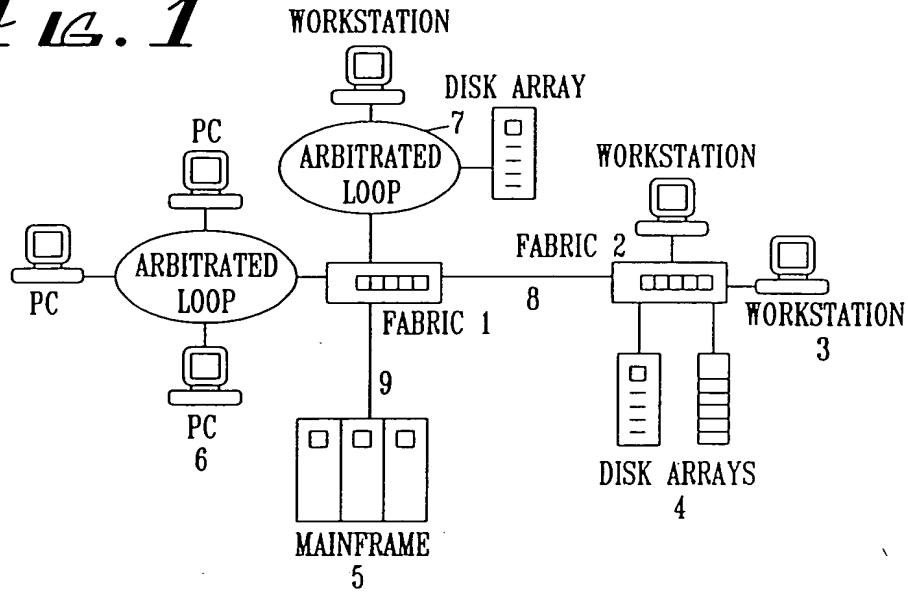


AMENDMENTS TO THE DRAWINGS:

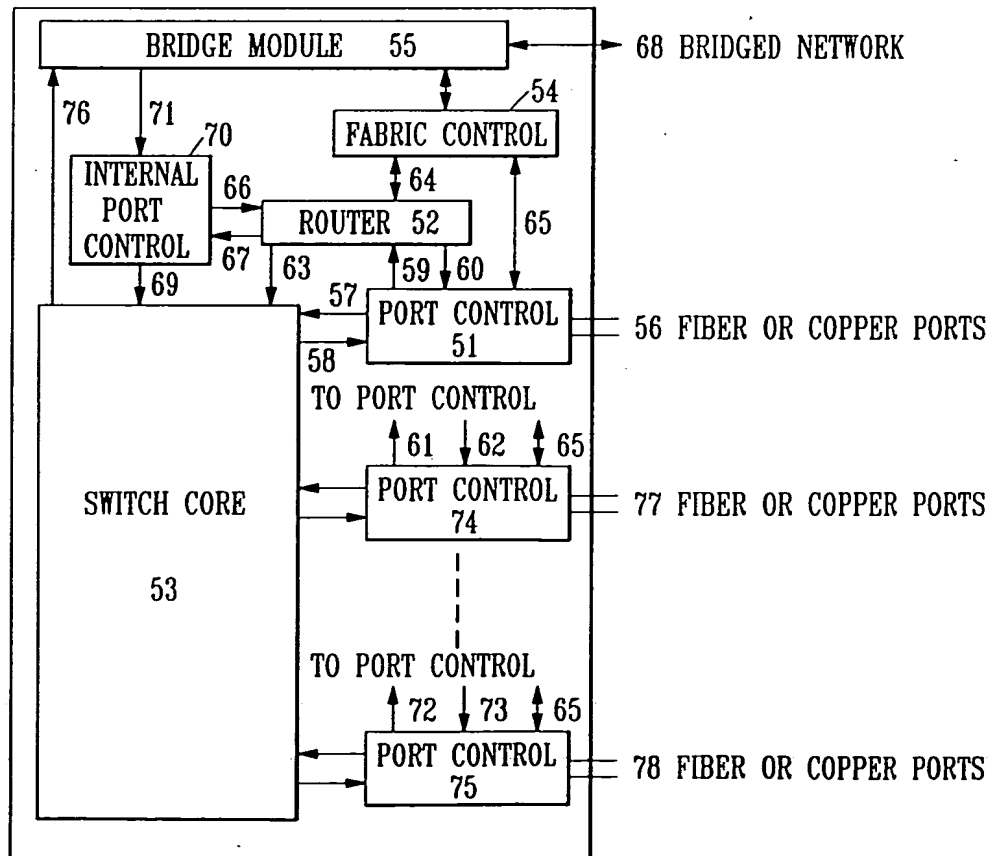
In response to the Notice of Draftperson's Patent Drawing Review attached to the Office Action dated June 20, 2003, Applicants provide formal drawings for the above-noted application. It is believed that these drawings are in compliance with the PTO rules.

Fig. 1



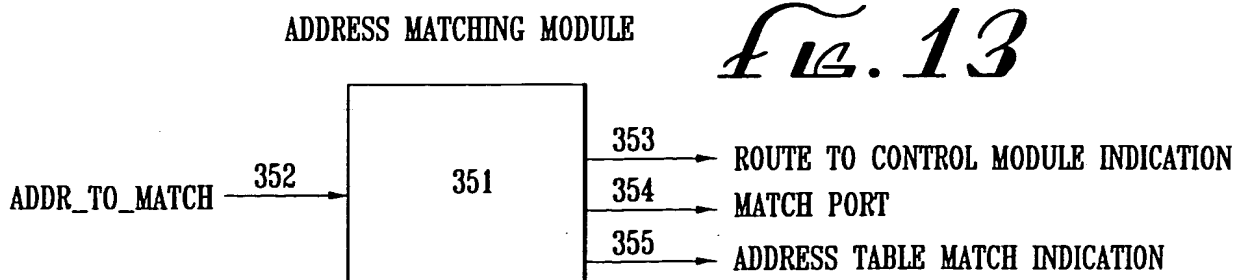
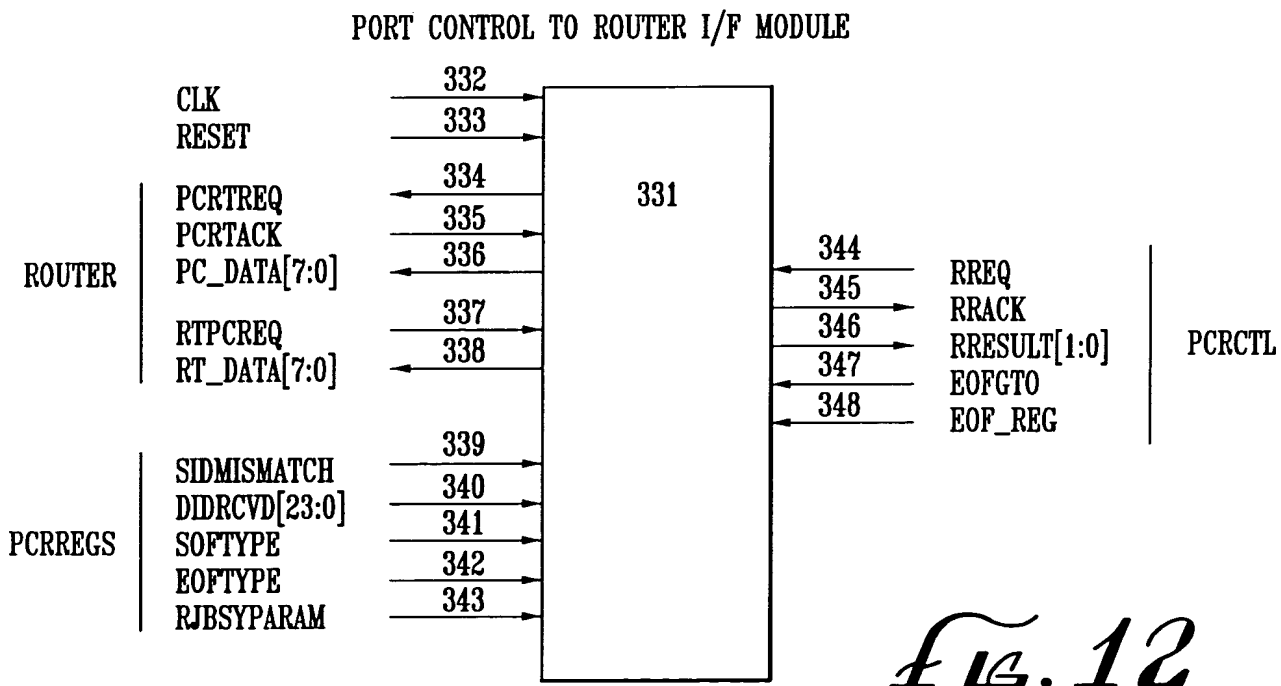
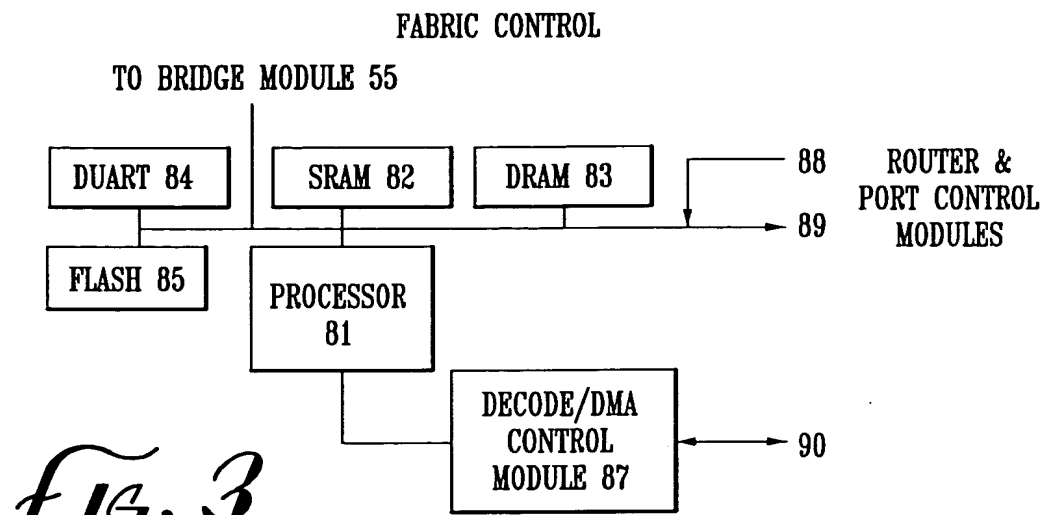
FIBRE CHANNEL FABRIC BLOCK DIAGRAM

Fig. 2

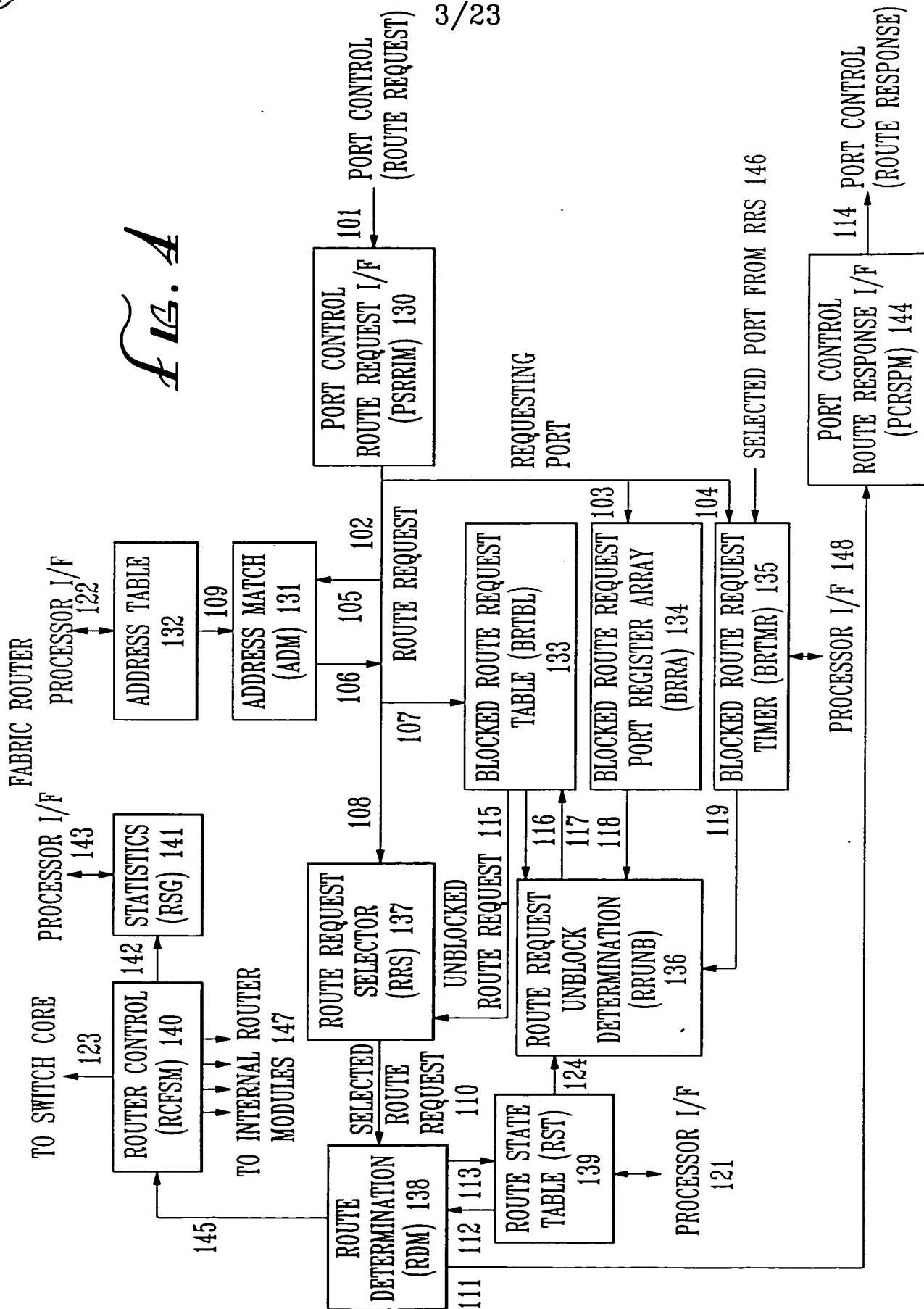




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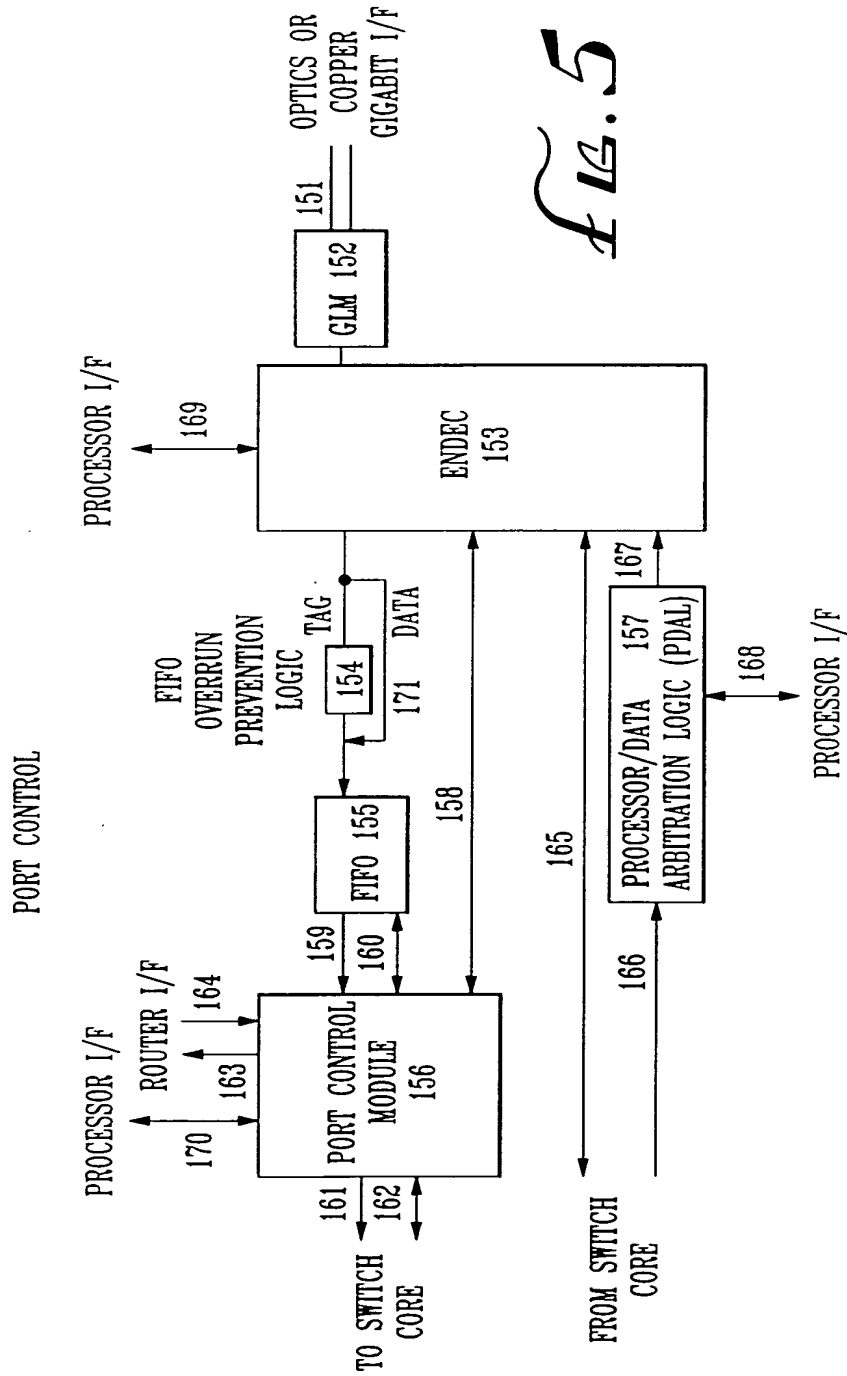


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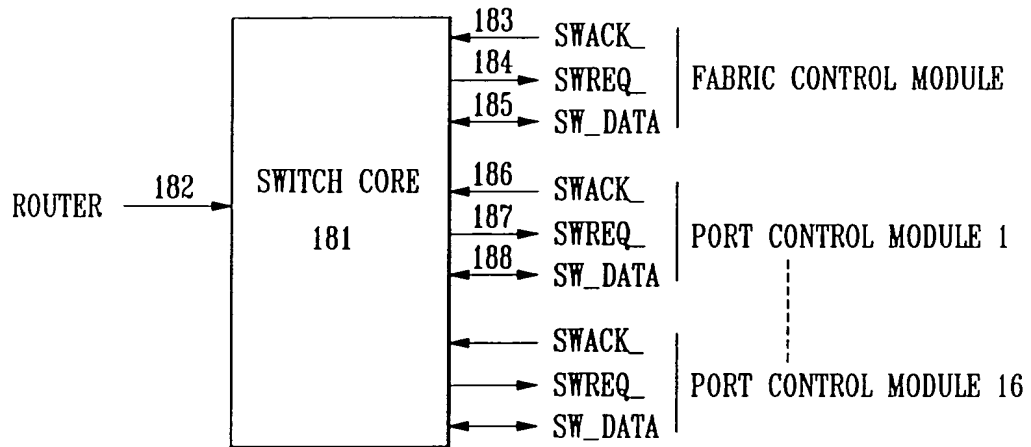


FIG. 6

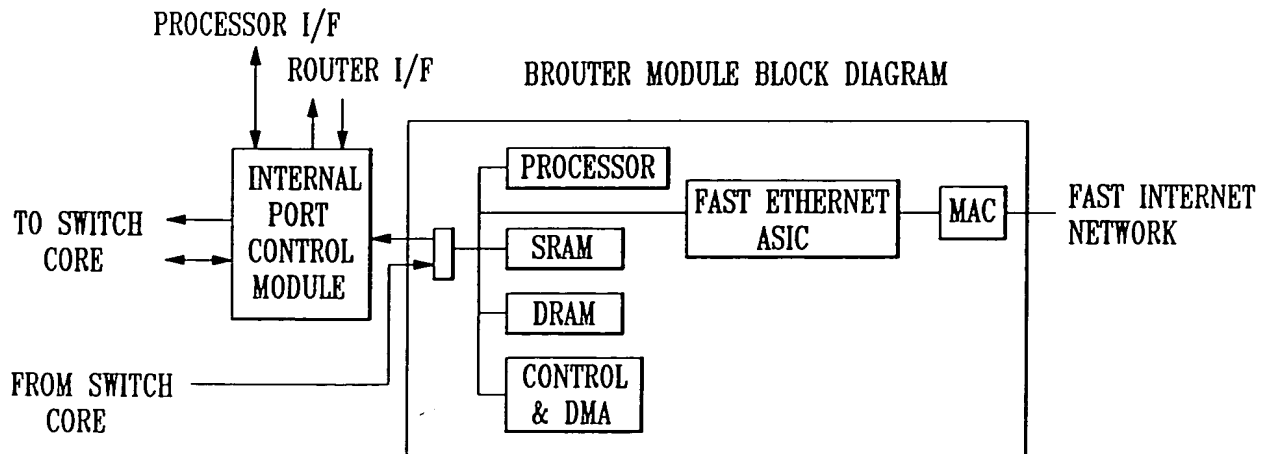


FIG. 7



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FIFO OVERRUN PREVENTION LOGIC

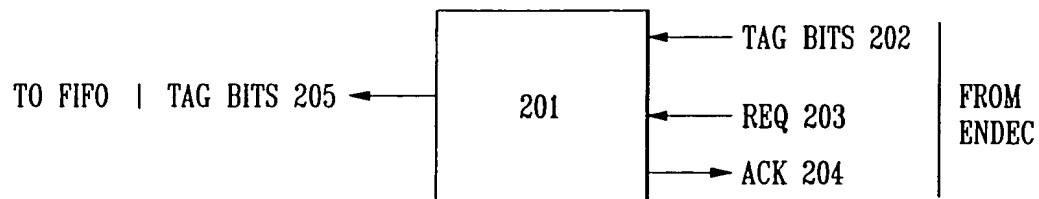


Fig. 8

PROCESSOR/ENDEC ARBITRATION LOGIC

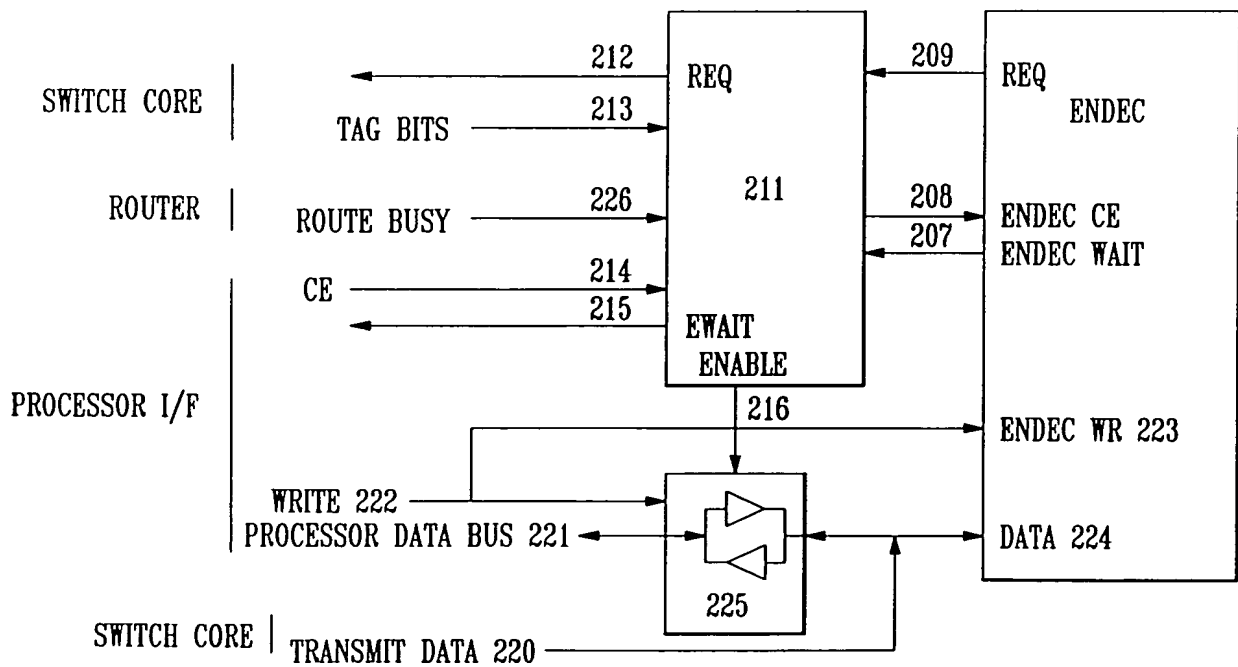


Fig. 9

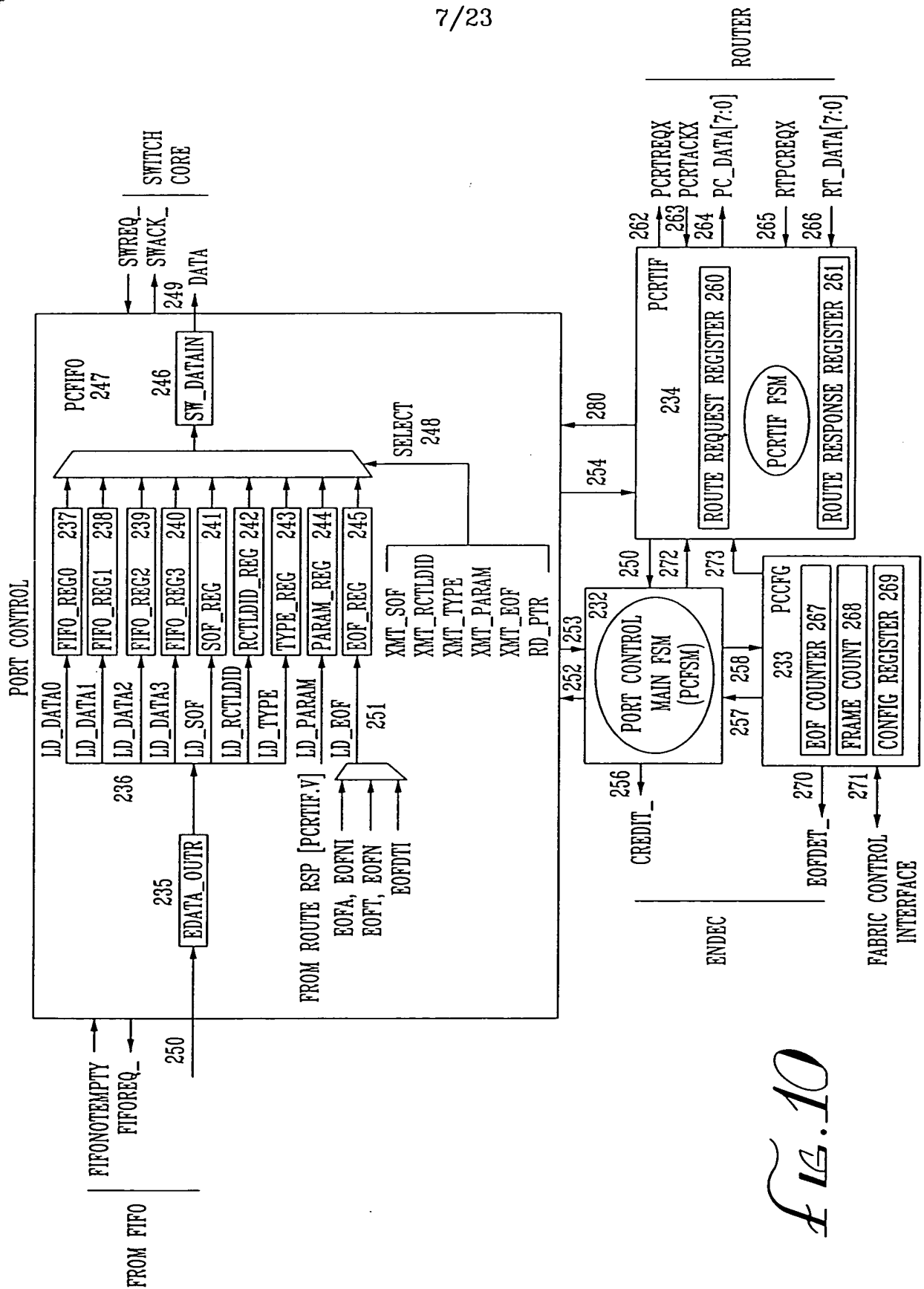
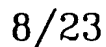


FIG. 10





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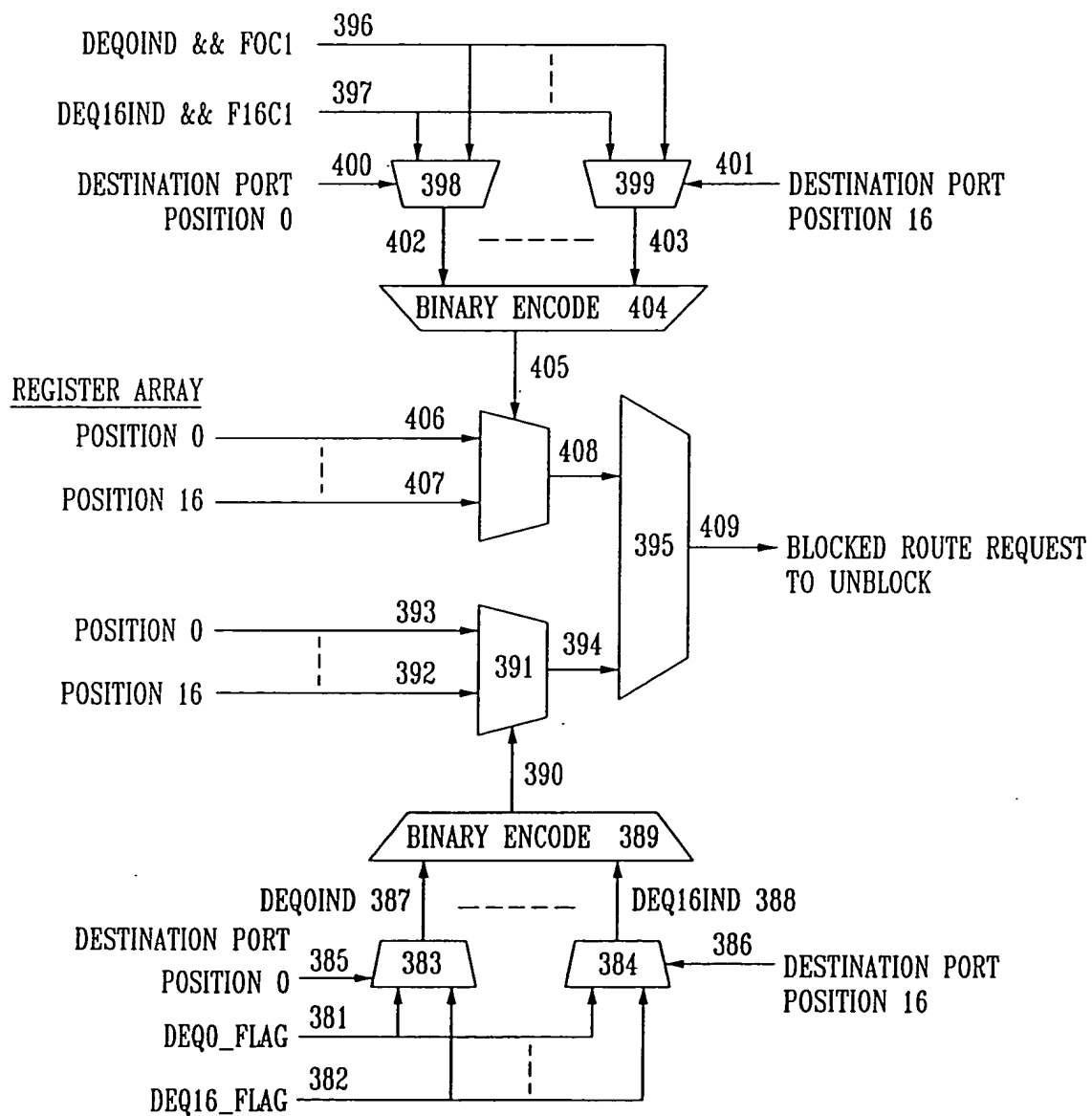


Fig. 15



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FROM ROUTE
STATE TABLE

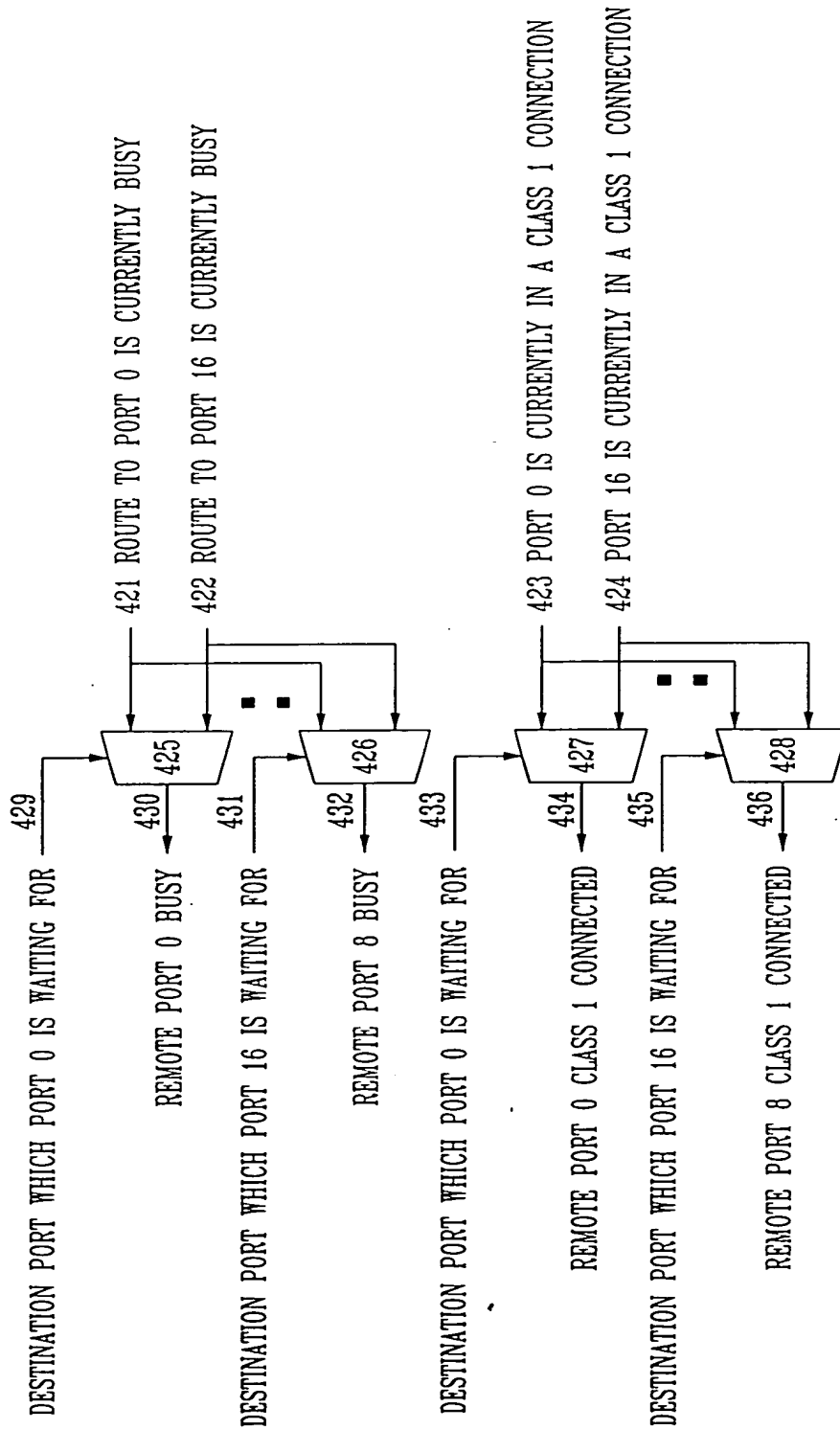
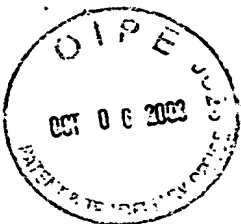


Fig. 10



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BLOCKED ROUTE REQUEST TABLE (BRTBL)

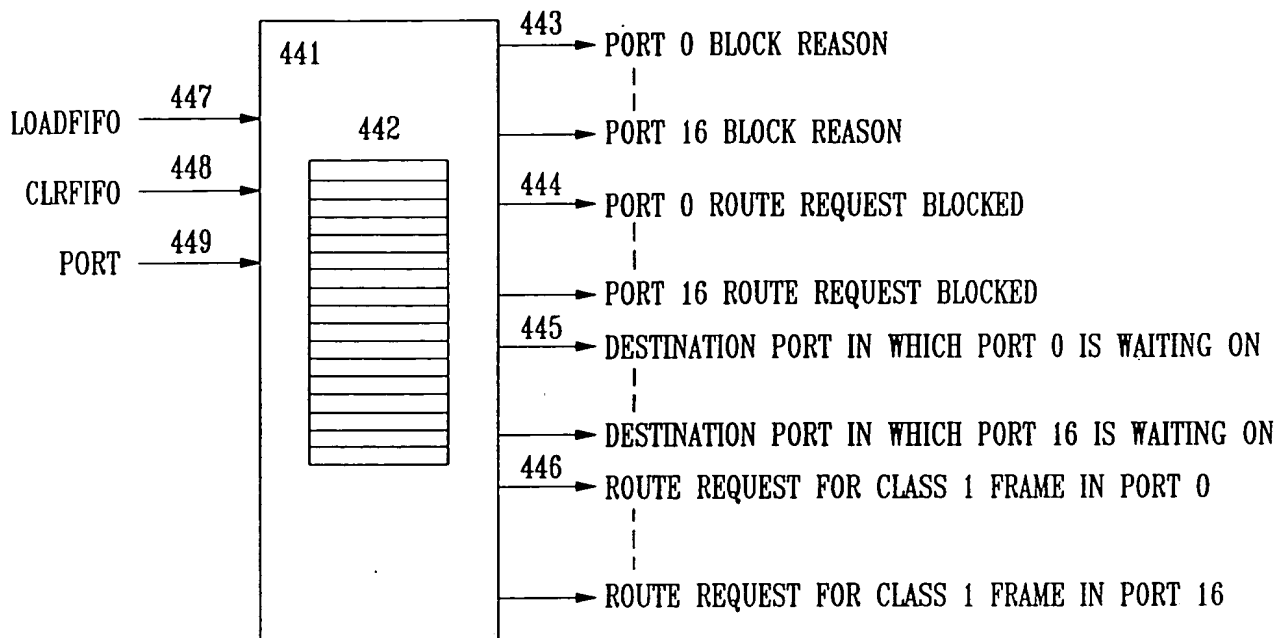


Fig. 17

BLOCKED ROUTE REQUEST PORT REGISTER ARRAY (BRR)

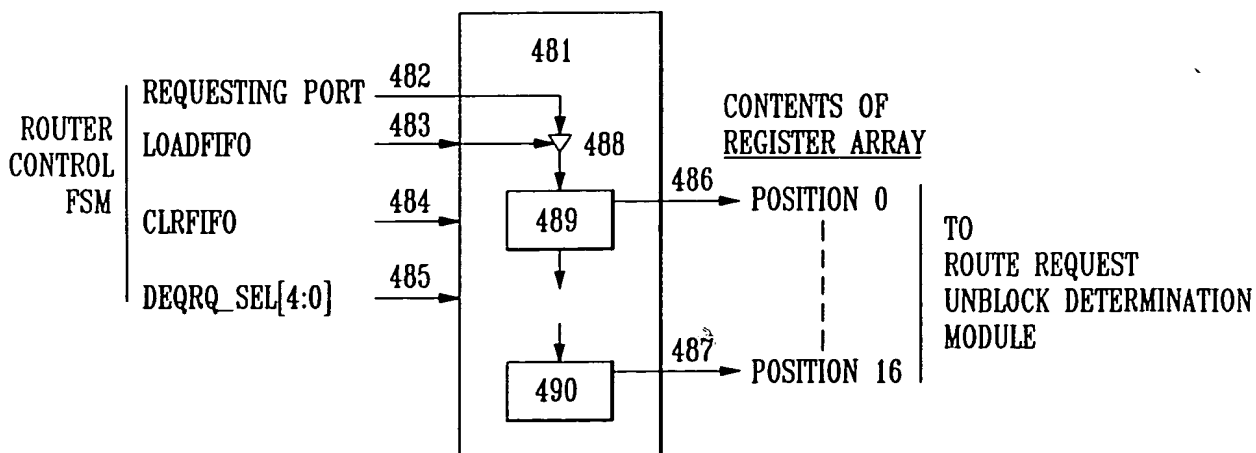
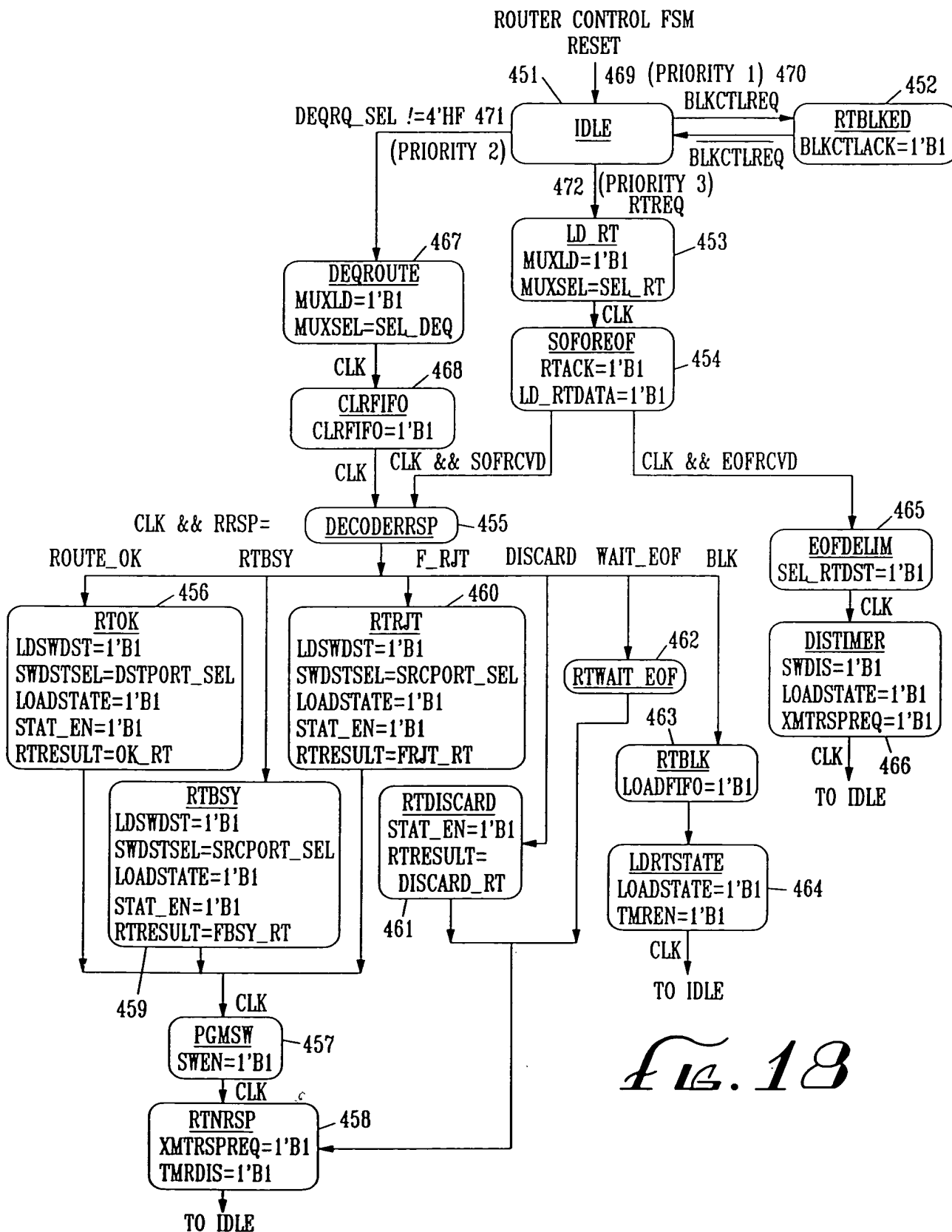


Fig. 19



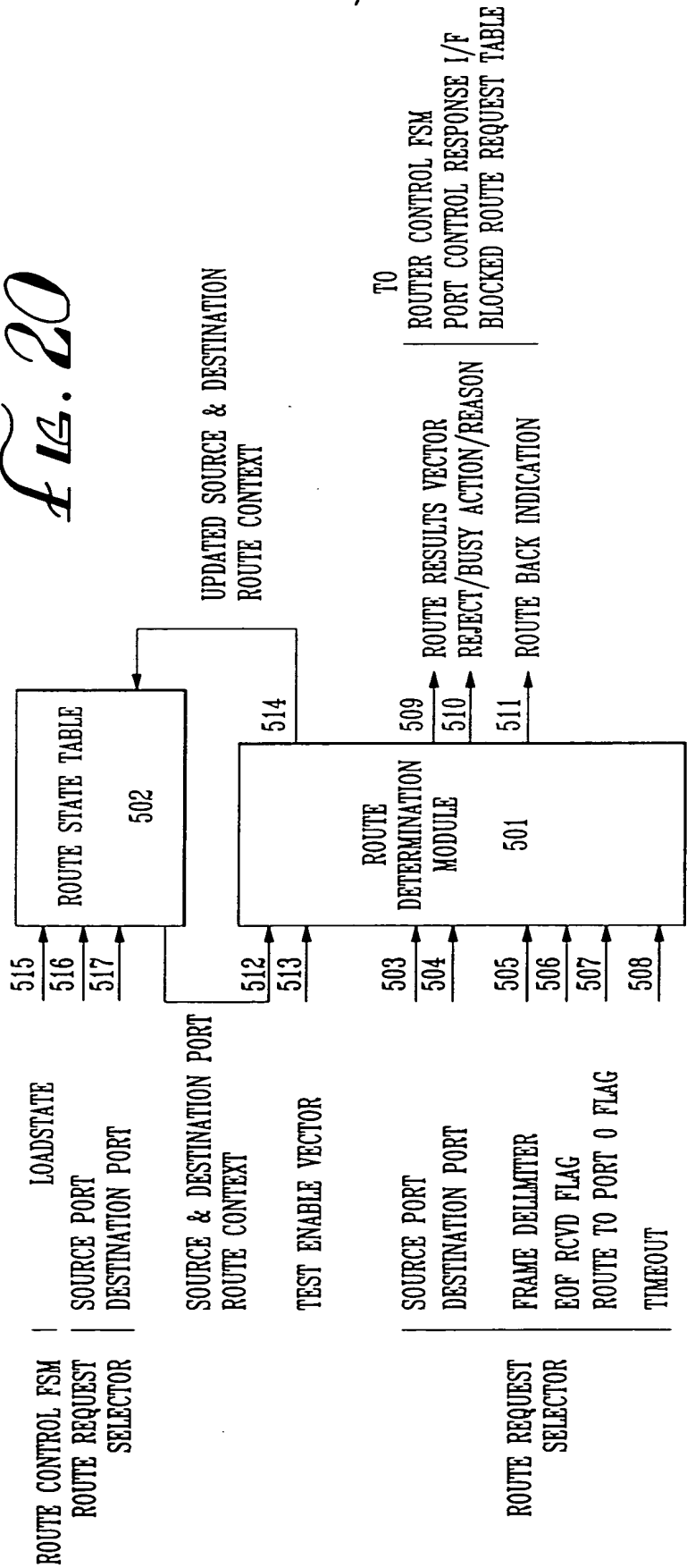
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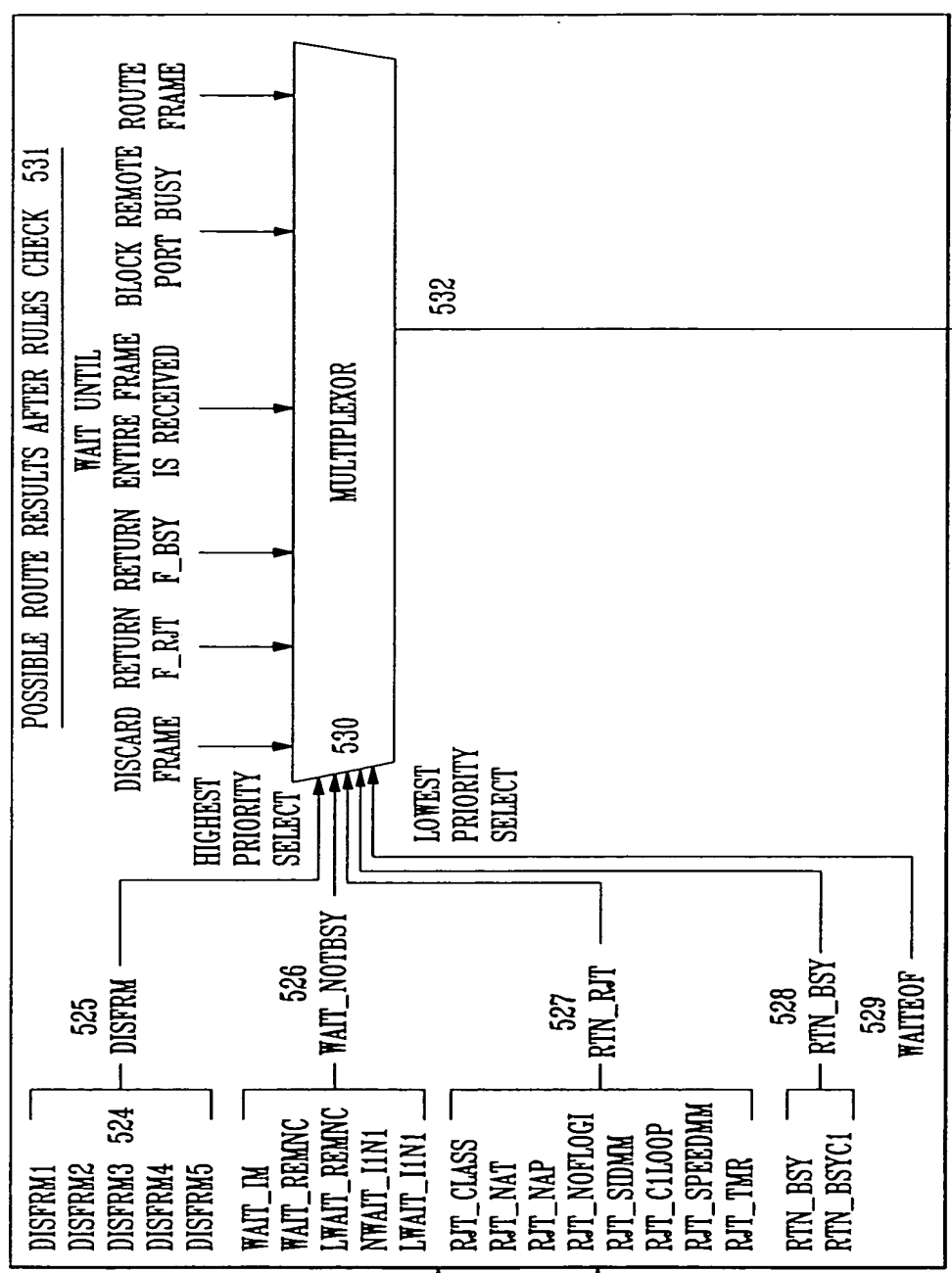
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Fig. 20





ROUTE DETERMINATION MODULE 521



ROUTING RESULTS

Fig. 21

INPUT SIGNALS

CONTEXT:

SOURCE PORT CONTEXT

DESTINATION PORT CONTEXT

SOURCE PORT

DESTINATION PORT

FRAME DELIMITER (SOF OR EOF)

BLOCKED REQUEST TIMEOUT FLAG

522

523



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ROUTE DETERMINATION MODULE

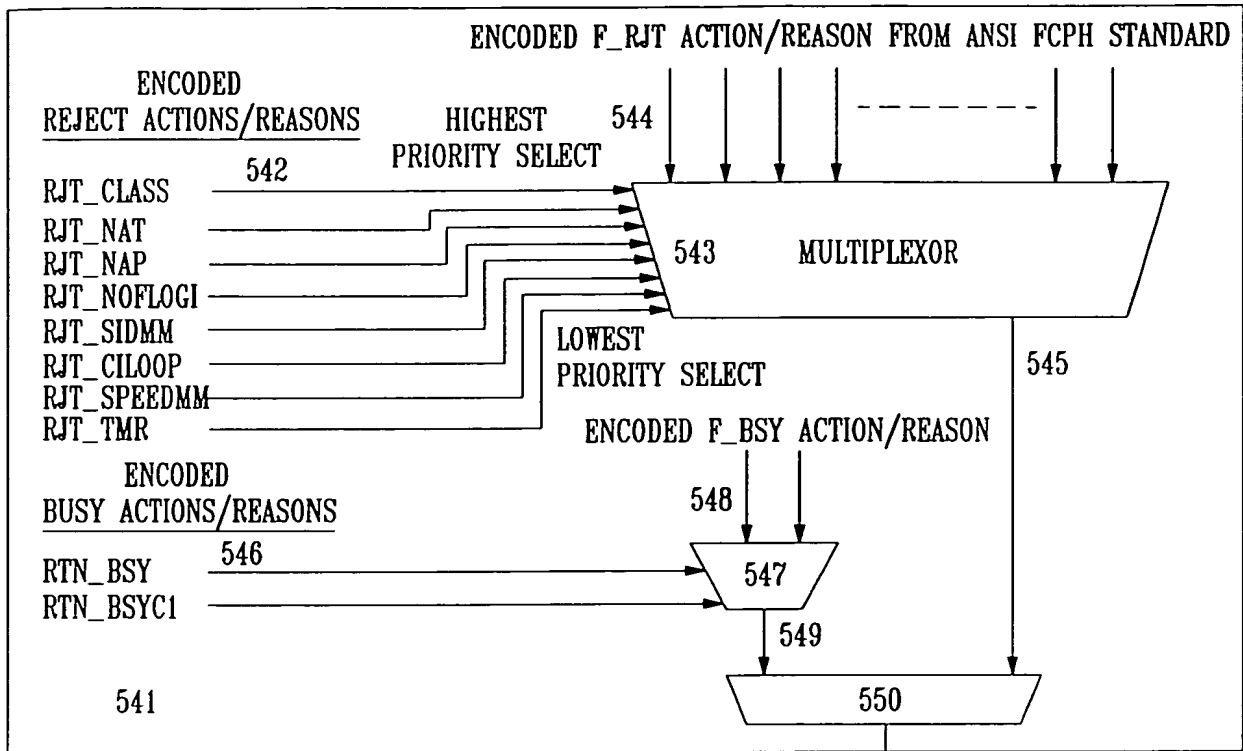


Fig. 22

ROUTE DETERMINATION MODULE

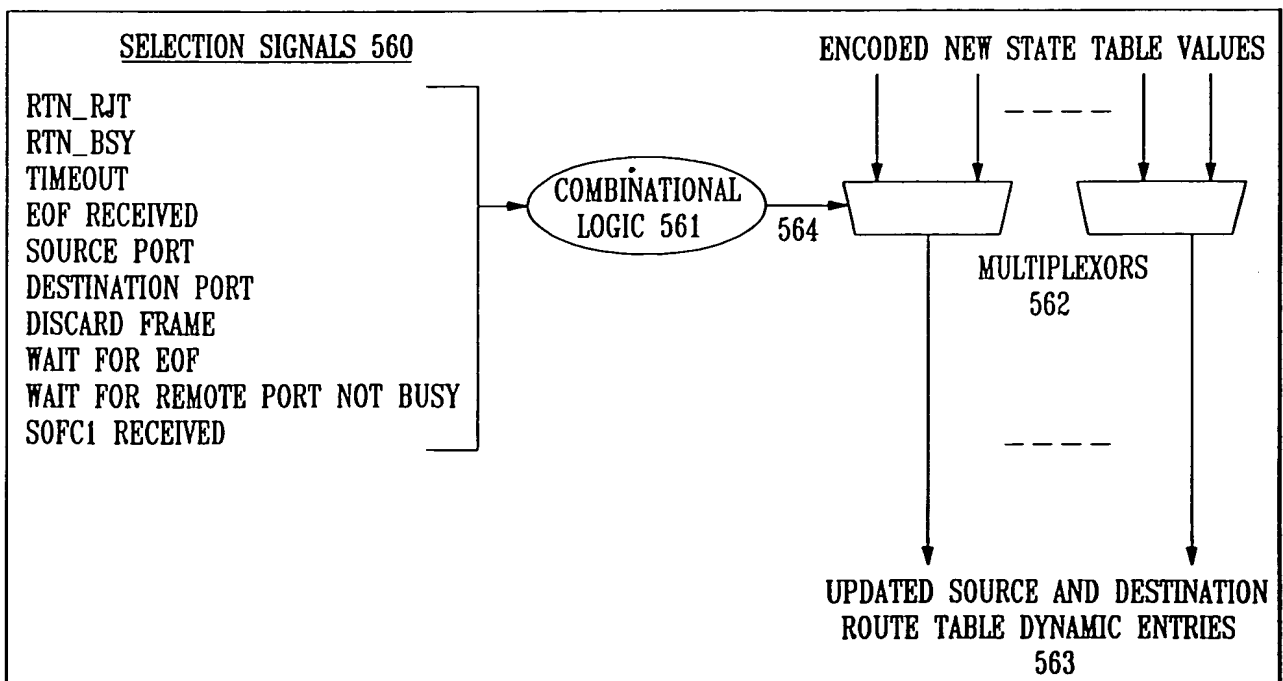


Fig. 23



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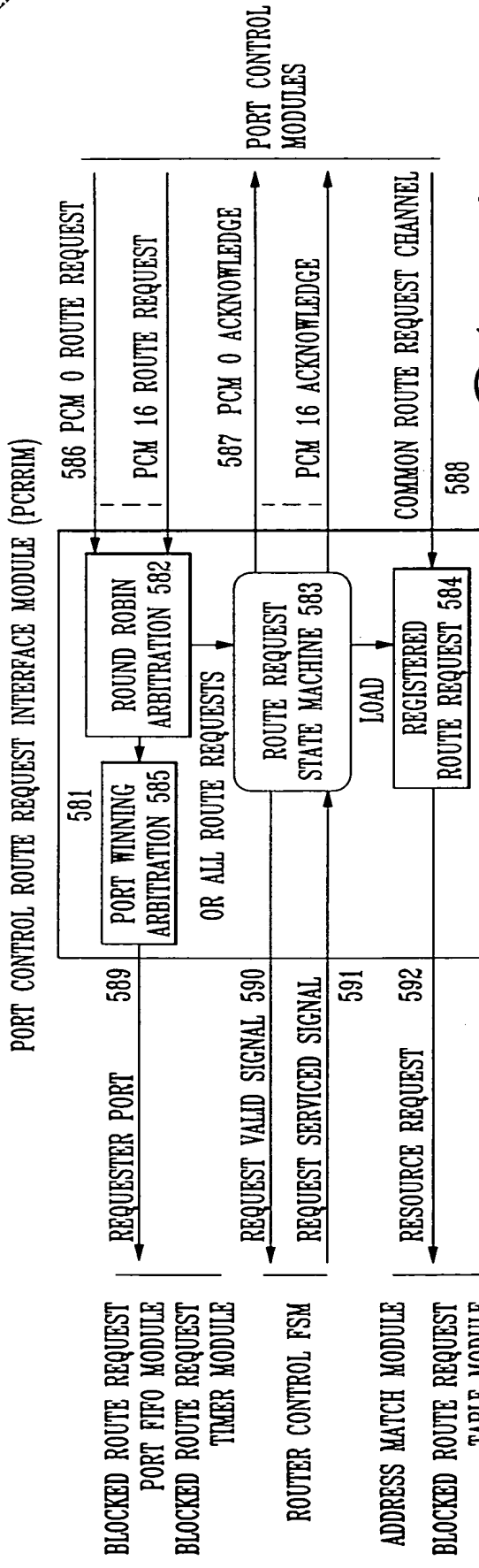


fig. 24

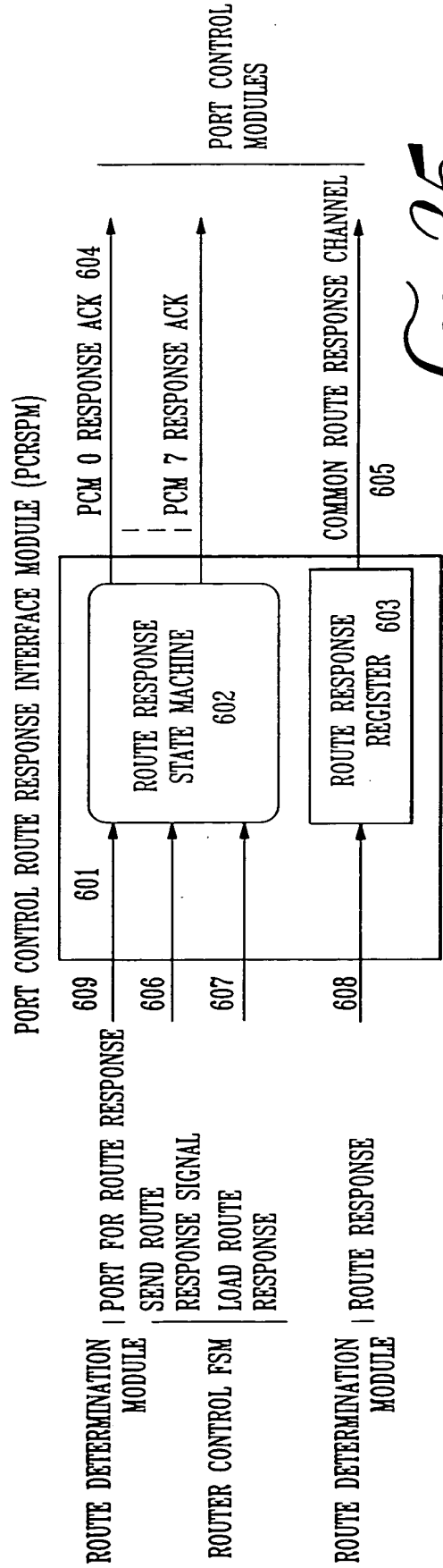


fig. 25



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ROUTER TO PORT CONTROL ROUTE REQUEST FSM (PCRRIM)

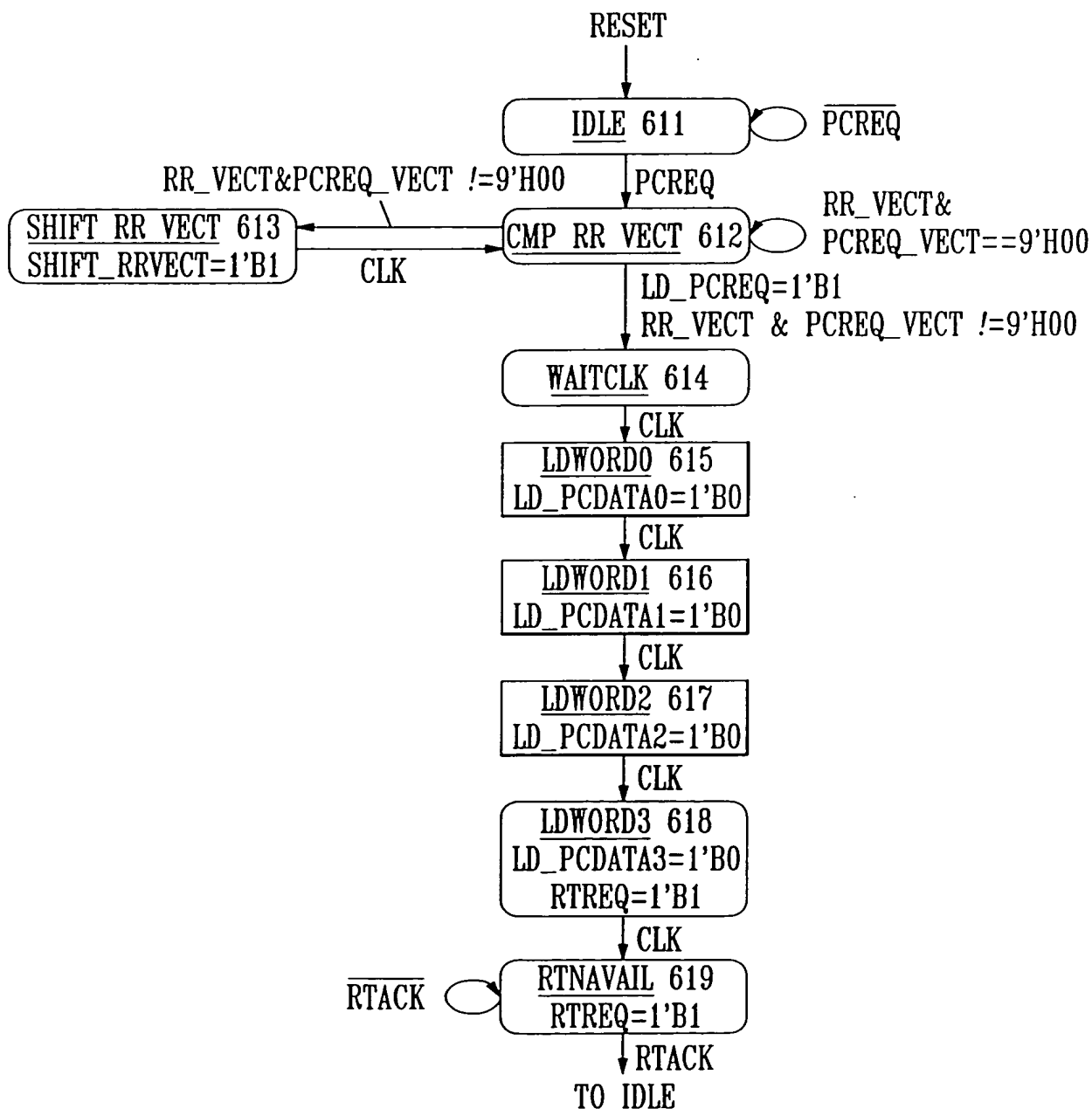


Fig. 20



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7

ROUTER TO PORT CONTROL ROUTE RESPONSE STATE MACHINE (PCRSPM)

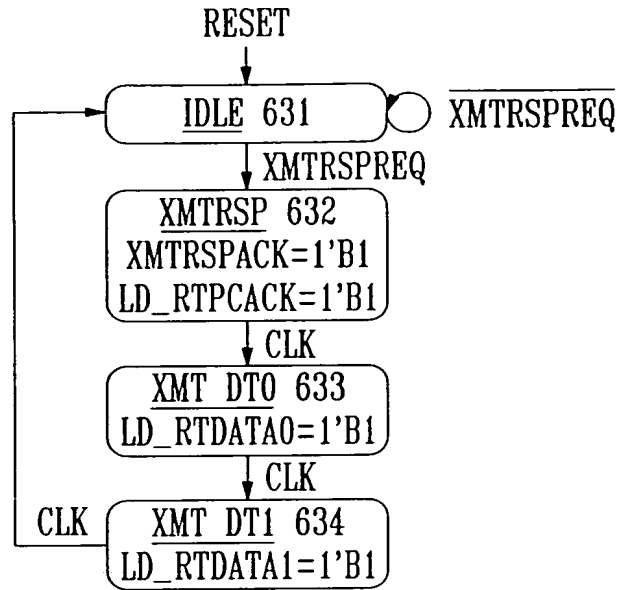


Fig. 27

BLOCKED ROUTE REQUEST TABLE ENTRY FORMAT

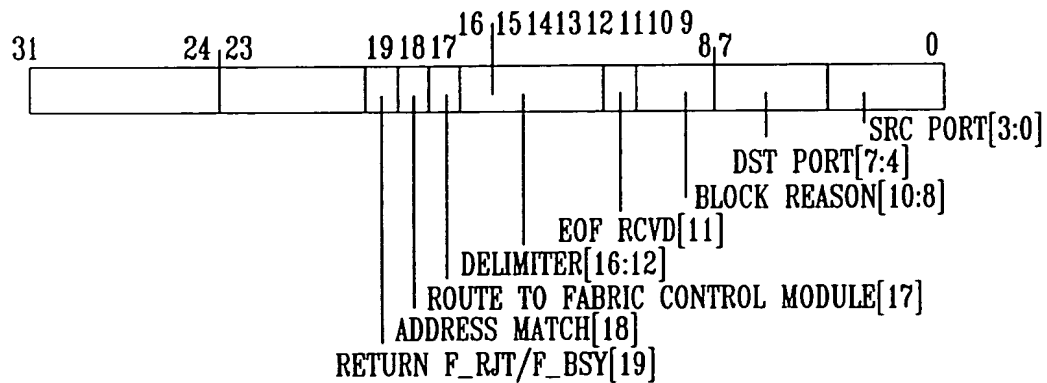


Fig. 30



PORT CONTROL TO ROUTER INTERFACE STATE MACHINE

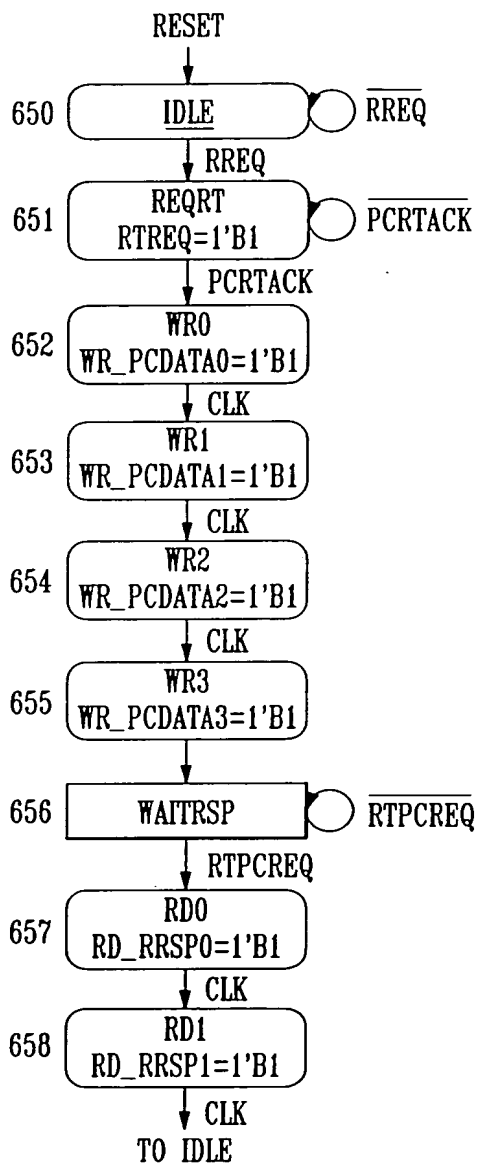


FIG. 28



PORT CONTROL HUB BLOCK DIAGRAM

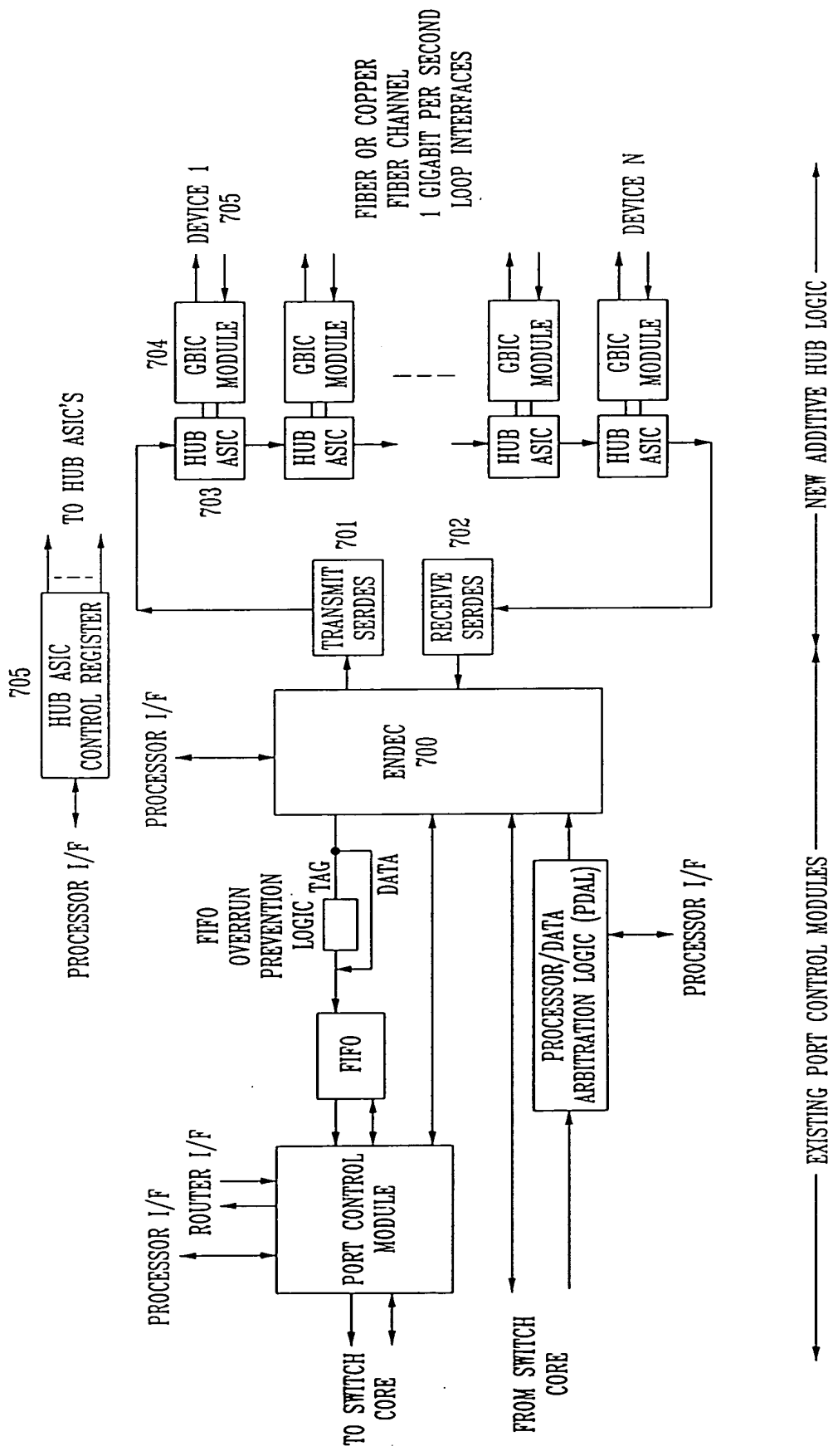
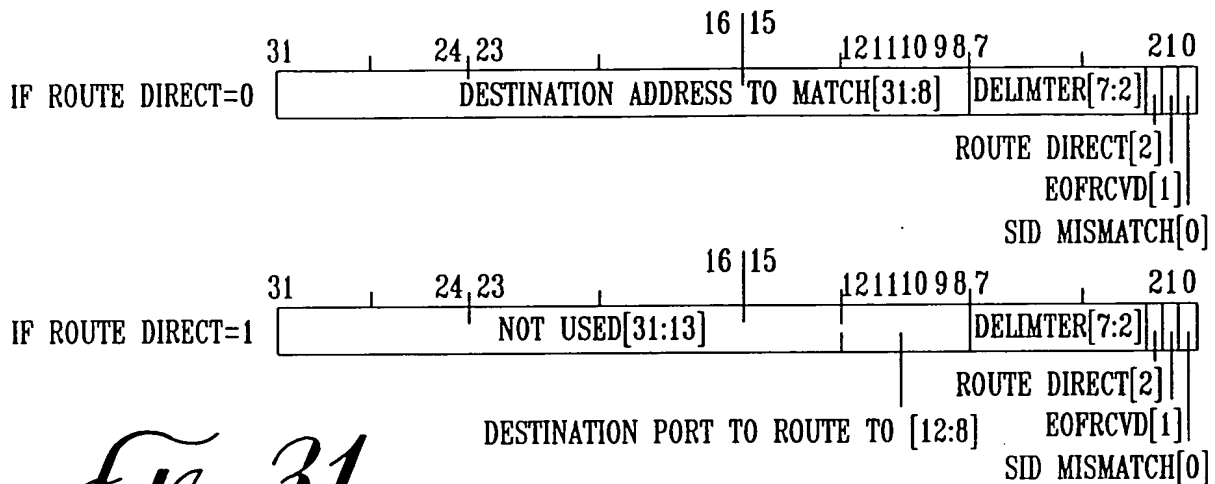


Fig. 29

ROUTE REQUEST FORMAT



f 16. 31

ROUTER TO PORT CONTROL RESPONSE FORMAT

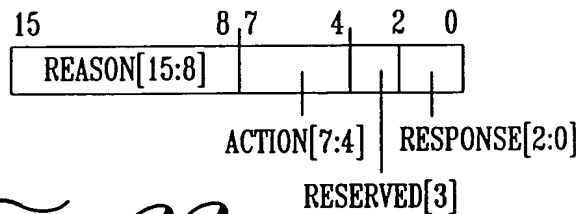
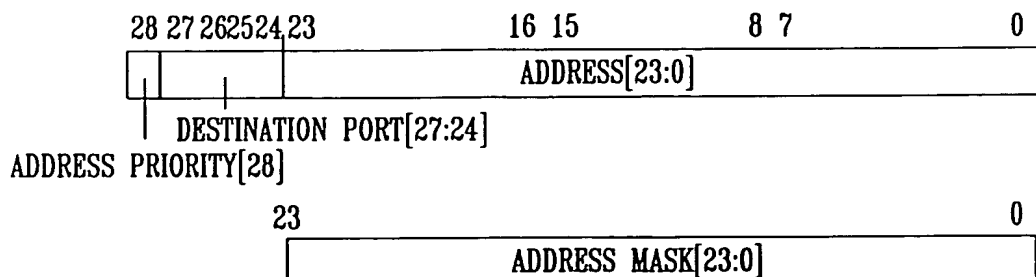


Fig. 32

ADDRESS TABLE ENTRY FORMAT

Fl. 33



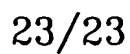


Figure 1 illustrates a 32-bit register structure, divided into two main sections: **STATIC (UPDATED BY THE FABRIC CONTROL MODULE)** and **DYNAMIC (UPDATED BY THE ROUTE DETERMINATION MODULE)**.

The register is organized as follows:

- Static Section (Bits 31-16):**
 - Bits 31-24: **NO USED**
 - Bit 23: **FLOGI OCCURRED[23]**
 - Bit 22: **INTERMIX SUPPORT[22]**
 - Bits 21-20: **PORT SPEED[21:20]**
 - Bit 19: **LOOP PORT INDICATION[19]**
- Dynamic Section (Bits 15-0):**
 - Bit 12: **PORT BUSY[12]**
 - Bits 15-13: **PORT STATED[15:13]**
 - Bits 18-16: **CLASS SUPPORTED[18:16]**
 - Bit 11: **CLASS 1 CONNECTION STATE[11]**
 - Bits 10-8: **TIMER STATE[10:8]**
 - Bits 7-4: **CLASS 1 DESTINATION CONNECT PORT[7:4]**
 - Bits 3-0: **DESTINATION PORT CONNECTED TO[3:0]**

fig. 34